

# Dual-polarization IMDD System for Data-Center Connectivity

Ying Zhao<sup>(1)</sup>, Christopher Doerr<sup>(1)</sup>, Fatemeh Ghaedi Vanani<sup>(2)</sup>, Makoto Takeshita<sup>(3)</sup>, Harold Kamisugi<sup>(4)</sup>

(1) Aloe Semiconductor, [yzhao@aloesemi.com](mailto:yzhao@aloesemi.com)

(2) University of Central Florida

(3) NTT Innovative Devices Corporation

(4) Sumitomo Electric Device Innovations, Inc.

**Abstract** A dual-polarization IMDD system is presented by multiplexing two polarizations in an EML based transmitter assembly and demultiplexing in a silicon photonics integrated receiver. A novel polarization recovery algorithm is the key enabler of the fast and robust polarization tracking. ©2024 The Author(s)

## Introduction

Hyperscale and AI-driven data centers spearhead fundamental changes in network architecture. As the need for higher-speed transmission is growing, photonic integration is leading the next technology transitions for inter- and intra-data-center connectivity, which enables higher density, higher yield, smaller footprint and lower cost.

Dual-polarization (DP) multiplexed transmission systems double the capacity of a single mode fiber (SMF). Unlike the coherent precedent which acquires optical field information and employs digital signal processing (DSP) for polarization demultiplexing, intensity modulation direct detection (IMDD) systems must perform an active polarization recovery before photodetection, because optical phase information is erased by the square-law detection. There have been previous efforts on DP-IMDD systems [1-5]. However, performance suitable for a real-world system was not fully demonstrated.

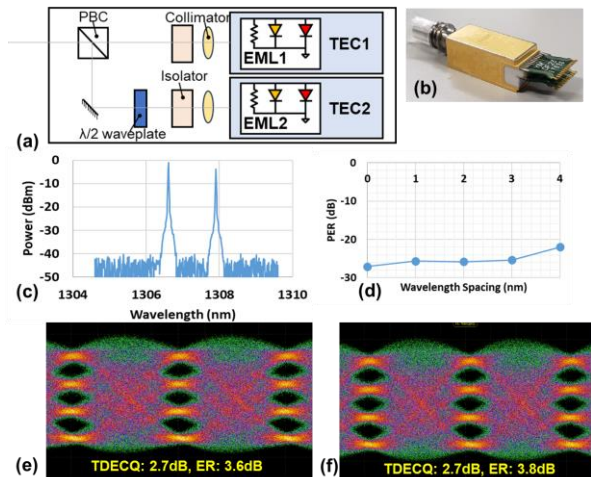
This paper focuses on the feasibility of a DP-IMDD system under various data-center practical constraints on reliability and cost.

On the device level:

- A DP externally modulated laser (EML) based transmitter optical sub assembly (TOSA) is presented, serving as an integrated solution for a DP transmitter (Tx).
- A silicon-photonics (SiPh) integrated receiver with active polarization control based on vectorized state-of-polarization (SOP) monitor is presented, serving as an integrated solution for a DP receiver (Rx).

On the system level:

- A robust, fast and endless polarization tracking algorithm is purposed and implemented, avoiding a multiple-step blind search or hill-climbing algorithm [6,7]. The implementation is based on a low-cost ARM processor.
- Realtime post-FEC transmission experiment shows codeword error-free with polarization scrambling or hand shaking, vibrating, and/or twisting the fiber link.



**Fig. 1:** DP EML TOSA (a) schematic diagram (b) package picture (c) optical spectrum of two output channels (d) PER versus wavelength spacing (e)(f) Eye diagram of two output channels

## DP EML TOSA

Fig. 1(a) shows the schematic diagram of the DP EML TOSA. Two EMLs are respectively mounted onto two thermo-electric coolers (TECs). Thermistors and monitor photodiodes (PDs) are incorporated to keep the laser temperature and output power constant. Spatial polarization multiplexing is comprised of beam collimators, isolators, a half-wave plate and a polarization beam combiner (PBC) [8]. A picture of the TOSA is shown in Fig.1 (b). Two flexible printed circuits (FPCs) are used for electrical connections with separated high-frequency and low-frequency signal paths. An LC receptacle incorporating a SMF is used for the optical output port. The dimensions of the device are 26.8 × 6.7 × 5.3 mm<sup>3</sup>.

The laser threshold current is ~12mA, and the fiber output power is 5mW for 80mA drive current. The DC extinction ratio (ER) is beyond 10dB for a reverse bias from -1V to -3V. Fig. 1(c) shows the optical spectrum. By tuning the TECs, EML1 is fixed at 1306.6nm and EML2 at 1307.9nm, with an offset of 1.3nm. Fig. 1(d) shows that the measured polarization extinction ratio (PER) is beyond 25dB, which guarantees good orthogonality

between two polarizations. The Tx polarization dependent loss (PDL) can be adjusted by the laser current and modulator reverse bias. In the experiment, the PDL is optimized within 0.5dB.

Figures 1(e) and (f) show the equalized 106.25Gbps eye diagram on each polarization respectively. EML1 shows a TDECQ of 2.7dB and ER of 3.6dB, and EML2 TDECQ of 2.7dB and ER of 3.8dB. Shorter RF interconnection between the TOSA and the DSP chip can potentially improve TDECQ and ER. This DP EML TOSA can be upgraded to 200Gbps per polarization.

### SiPh DP Rx

As shown in Fig. 2(a), a monolithically integrated SiPh DP Rx is comprised of a polarization demultiplexer, a tapped vectorized SOP monitor and two high-speed silicon-germanium PDs. Fig. 2(b) shows a picture of the SiPh die. The size is  $5.8 \times 1.5 \text{ mm}^2$ .

The polarization demultiplexer serves the function of polarization recovery. The received DP signal is split and converted into two tributaries of transverse electric (TE) mode signal after the polarization beam splitter and rotator (PBSR). An endless control stage is employed to allow continuous tracking even if the following phase shifters hit their control limit [9]. Following the endless control stage, two cascaded Mach-Zehnder interferometers (MZIs), with the controlling phase  $\phi$  and  $\theta$ , act as a unitary polarization controller that can convert any input SOP to the desired demultiplexed SOP [10]. The analytical solution of  $\phi$  and  $\theta$ , which is critical to guide the tracking algorithm, is presented in the following section. The bandwidth of the thermally controlled phase shifter is beyond 30kHz.

The tapped SOP monitor, which is implemented based on optical hybrids and low-speed PDs, has a tap ratio less than 5% and a bandwidth less than 1GHz. The vectorized output signal from the monitor, denoted by  $\vec{e} = [e_1, e_2, e_3]^T$ , incorporates both optical amplitude and phase information, so that can fully characterize the SOP at the tapped point.

The silicon-germanium PD is able to support 200Gbps per polarization, so the DP Rx potentially supports 400Gbps per fiber.

### Polarization Recovery Algorithm

Unlike previous polarization tracking schemes [1-3,6,7], which mainly employ blind search or hill-climbing algorithms, we use a vectorized SOP monitor  $\vec{e}$  for polarization demultiplexing. Under the assumption that device and link PDL are negligible, a unitary polarization transformation can be fully characterized by  $\vec{e}$ . Without losing generality,  $\vec{e}$  can be expressed in Stokes space. Since

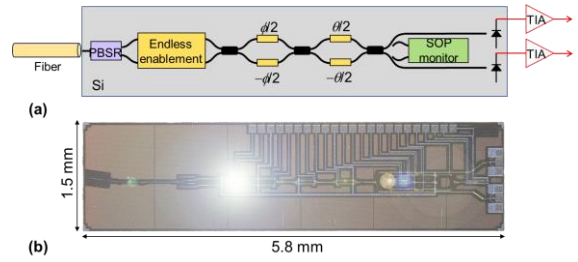


Fig. 2: SiPh DP Rx (a) block diagram (b) die picture

the unitary transformation maintains the orthogonality between two polarizations, the instantaneous monitored SOP of the modulated data forms a straight line passing through the origin and pointing to two opposite (orthogonal) points on the Poincare sphere. If the instantaneous S parameter is denoted by a  $3 \times N$  matrix  $\mathbf{S}_{3 \times N}$ , where  $N$  is the number of sampling point,  $\vec{e}$  can be expressed by the maximal eigenvector of the covariance matrix  $\mathbf{M}_{3 \times 3} = \mathbf{S}_{3 \times N} \cdot \mathbf{S}_{N \times 3}^T$ , which corresponds to the largest variance direction of the instantaneous SOP, so called the vectorized monitor SOP.

The vectorized SOP can be used to guide the controlling phase  $\phi$  and  $\theta$  to achieve polarization demultiplexing. The closed form of the solution of the demultiplexing phase  $\phi^*$  and  $\theta^*$  can be expressed by

$$\phi^* = \text{atan} \left( \frac{d_3}{d_2} \right) \quad \text{Eq.(1a)}$$

$$\theta^* = \text{atan} \left( \frac{d_2 \cos(\phi^*) + d_3 \sin(\phi^*)}{d_1} \right) \quad \text{Eq.(1b)}$$

where  $\vec{d} = [d_1, d_2, d_3]^T = \mathbf{R} \cdot \vec{e}$  and  $\mathbf{R}$  is the unitary rotation matrix determined by the current value of the controlling phase  $\phi$  and  $\theta$ , expressed by

$$\mathbf{R}(\phi, \theta) = \begin{pmatrix} -\cos(\theta) & -\cos(\phi) \sin(\theta) & -\sin(\phi) \sin(\theta) \\ -\sin(\theta) & \cos(\phi) \cos(\theta) & \sin(\phi) \cos(\theta) \\ 0 & \sin(\phi) & -\cos(\phi) \end{pmatrix} \quad \text{Eq. (2)}$$

The analytical solution of the controlling phase enables a one-step polarization recovery for any random input SOP, which is desirable for fast and accurate polarization tracking. Eq. (1) is implemented in an ARM MCU with 170MHz Cortex-M4 core, and trigonometric functions are accelerated using common microcontroller software interface standard (CMSIS) DSP library [11].

An auxiliary endless control portion is implemented to avoid  $\phi$  and  $\theta$  running out of range [9].

### Transmission Experiment

As shown in Fig. 3, the transmission experiment setup incorporates the DP EML TOSA and SiPh DP Rx. The DP EML TOSA is connected to an evaluation board through the FPC and driven by

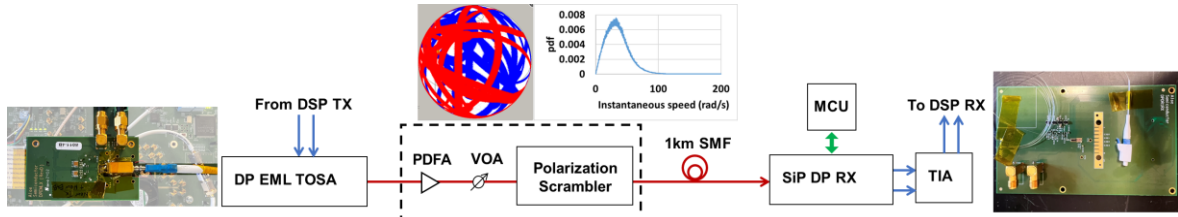


Fig. 3: Experimental setup of 1km  $2 \times 106.25$ Gbps DP transmission

2 of 4 channels from a Broadcom Centenario 87400 DSP evaluation board with the line rate of 106.25Gbps. The DP Rx PIC is wire bonded to a Macom transimpedance amplifier (TIA), 2 channels of which are connected to a DSP evaluation board to collect real-time bit error rate (BER). 1km SMF is used as a transmission link to emulate an intra-data-center application. A polarization scrambler is inserted in the link to generate random polarization rotations to evaluate the demultiplexing performance. A praseodymium-doped fiber amplifier (PDFA) and a variable optical attenuator (VOA) are used to compensate extra loss from the scrambler and device.

For a static polarization case without turning on the scrambling, Fig. 4 shows the Rx PD sensitivity comparison between a single polarization (SP) setup and a DP setup. The single polarization setup is configured by shutting off one channel of the DP EML Tx and monitoring one channel BER from the DP Rx. It is shown that both SP and DP can achieve  $\sim 10^{-7}$  BER floor and  $\sim -8$ dBm sensitivity at  $2.4 \times 10^{-4}$  KP4 FEC threshold. The performance difference between SP and DP is negligible, which proves the feasibility of the DP-IMDD scheme.

In a dynamic scrambling case, the random polarization trajectory is visualized on Poincaré sphere as shown in the inset of Fig. 3. The scrambling speed is depicted by an instantaneous angular speed histogram, which shows a maximal speed of  $\sim 100$ rad/s. Figures 5(a) and (b) show the BER of two Rx channels over time up to 2 minutes with the dynamic scrambling on. Both channels show stable BER of  $\sim 10^{-7}$  level on LSB and MSB. Fig. 6(a) and (b) show the dynamic sampling of the controlling phase  $\phi$  and  $\theta$ , vectorized SOP monitor  $e_1, e_2, e_3$ . It can be seen that when the controlling phase keep tracking the input SOP change, the vectorized SOP can be maintained relatively stable.

A post-FEC experiment is performed by tuning on the KP4 FEC encoder and decoder on the line side. With random scrambling or with hand shaking, vibrating or twisting the fiber, there is no codeword error observed in 2 minutes and the reported KP4 FEC T-max did not exceed 4.

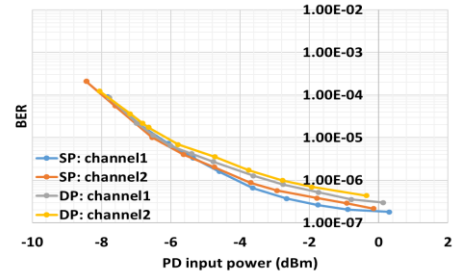


Fig. 4: PD sensitivity comparison between SP and DP

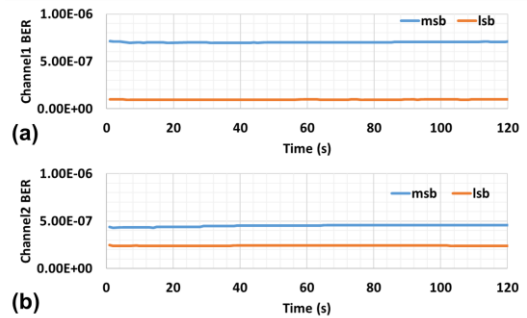


Fig. 5: Rx BER over time with polarization scrambling (a) Channel1 and (b) Channel2

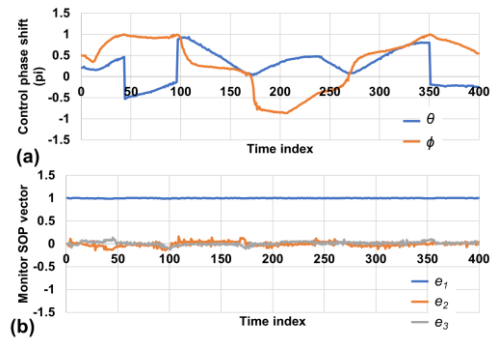


Fig. 6: (a) Controlling phase and (b) SOP Monitor over time

## Conclusions

This paper demonstrates a DP-IMDD transmission system by employing a DP EML TOSA as the Tx and a SiPh PIC as the Rx. By implementing the proposed fast converging polarization recovery algorithm, a  $2 \times 106.25$ -Gbps DP signal is successfully demultiplexed in a dynamic scrambling case. The experiment proves the feasibility of low-cost DP solution for intra-data-center applications. The scheme can potentially be applied on a  $2 \times 212.5$ -Gbps system, EML or SiPh Tx-based, paving the way for 400-Gbps IMDD short reach transmission with existing SERDES.

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